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AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Original) A modulator that receives a digital baseband signal and modulates the digital baseband signal to a quadrature modulated output signal, the modulator comprising:

a quadrature modulator compensation signal processor (QMCSP) adapted to receive the digital baseband signal, where the QMCSP includes a first digital filter to generate a digital compensated signal so that the digital compensated signal negates at least a portion of a quadrature impairment in an analog quadrature modulator system (AQMS) for a plurality of baseband frequencies;

the AQMS, where the AQMS is adapted to receive the digital compensated signal and a local oscillator signal, where the AQMS is further adapted to quadrature modulate, in analog domain, the digital compensated signal to the quadrature modulated output signal;

a termination switch adapted to provide an observation signal, where the termination switch is coupled to a sample signal related to the quadrature modulated output signal and coupled to a source for a ground signal, where the termination switch further switches between the sample signal and the source for the ground signal in response to a ground switch control signal;

a variable phase shifter adapted to receive the local oscillator signal and to provide a phase shifted output signal, where the phase shifted output signal is selectable to at least 3 phase shifts, and where a phase shift is selected in response to a phase shifter control signal;

an analog quadrature demodulator system (AQDS) adapted to receive the observation signal and the phase shifted output signal, the AQDS adapted to demodulate the observation signal and to recover a received baseband signal that is related to the baseband signal, and where the received baseband signal includes quadrature impairment;

a quadrature demodulator compensation signal processor (QDCSP) adapted to receive the received baseband signal from the AQDS, where the QDCSP includes a second digital filter to generate a demodulated baseband signal such that at least a portion

of the quadrature impairment added to the received baseband signal by the AQDS is compensated in the demodulated baseband signal for a plurality of frequencies; and

an adaptive control processing and compensation estimation (ACPCE) circuit adapted to monitor the baseband signal and the received baseband signal, where the ACPCE circuit is further adapted to update parameters used by the QMCSP and the QDCSP to compensate for quadrature impairment.

2. (Original) The modulator as defined in Claim 1, wherein the first digital filter of the QMCSP further comprises:

a first finite impulse response (FIR) filter adapted to receive an in-phase portion of the baseband signal and to generate a first in-phase portion of the digital compensated signal;

a second FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a second in-phase portion of the digital compensated signal;

a third FIR filter adapted to receive an in-phase portion of the baseband signal and to generate a first quadrature-phase portion of the digital compensated signal;

a fourth FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a second quadrature-phase portion of the digital compensated signal;

a first summing circuit adapted to combine the first in-phase portion of the digital compensated signal with the second in-phase portion of the digital compensated signal to generate an in-phase digital compensated signal; and

a second summing circuit adapted to combine the first quadrature-phase portion of the digital compensated signal with the second quadrature-phase portion of the digital compensated signal to generate a quadrature-phase digital compensated signal, where the in-phase digital compensated signal and the quadrature-phase digital compensated signal comprise the digital compensated signal.

3. (Original) The modulator as defined in Claim 2, wherein the first digital filter of the QMCSP further comprises:

a first register adapted to store a first value, and where the first summing circuit is further configured to combine the first value with the first and the second in-phase

portions of the digital compensated signal to generate the in-phase portion of the digital compensated signal; and

a second register adapted to store a second value, and where the second summing circuit is further configured to combine the second value with the first and the second quadrature-phase portions of the digital compensated signal to generate the quadrature-phase portion of the digital compensated signal.

4. (Original) The modulator as defined in Claim 1, wherein the first digital filter of the QMCSP further comprises:

a first finite impulse response (FIR) filter adapted to receive an in-phase portion of the baseband signal and to generate an in-phase digital compensated signal;

a second FIR filter adapted to receive an in-phase portion of the baseband signal and to generate a first quadrature-phase portion of the digital compensated signal;

a third FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a second quadrature-phase portion of the digital compensated signal; and

a summing circuit adapted to combine the first quadrature-phase portion of the digital compensated signal with the second quadrature-phase portion of the digital compensated signal to generate a quadrature-phase digital compensated signal, where the in-phase digital compensated signal and the quadrature-phase digital compensated signal comprise the digital compensated signal.

5. (Original) The modulator as defined in Claim 1, wherein the first digital filter of the QMCSP further comprises:

a first finite impulse response (FIR) filter adapted to receive an in-phase portion of the baseband signal and to generate a first in-phase portion of the digital compensated signal;

a second FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a second in-phase portion of the digital compensated signal;

a third FIR filter adapted to receive a quadrature-phase portion of the baseband signal and to generate a quadrature-phase digital compensated signal; and

a summing circuit adapted to combine the first in-phase portion of the digital compensated signal with the second in-phase portion of the digital compensated signal to

generate an in-phase digital compensated signal, where the in-phase digital compensated signal and the quadrature-phase digital compensated signal comprise the digital compensated signal.

6. (Original) The modulator as defined in Claim 1, wherein the QDCSP is implemented in firmware.

7. (Original) The modulator as defined in Claim 1, wherein the second digital filter of the QDCSP further comprises:

a first FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate a first in-phase portion of the demodulated baseband signal;

a second FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a second in-phase portion of the demodulated baseband signal;

a third FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate a first quadrature-phase portion of the demodulated baseband signal;

a fourth FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a second quadrature-phase portion of the demodulated baseband signal;

a first summing circuit adapted to combine the first in-phase portion of the demodulated baseband signal with the second in-phase portion of the demodulated baseband signal to generate an in-phase demodulated baseband signal; and

a second summing circuit adapted to combine the first quadrature-phase portion of the demodulated baseband signal with the second quadrature-phase portion of the demodulated baseband signal to generate a quadrature-phase demodulated baseband signal, where the in-phase demodulated baseband signal and the quadrature-phase demodulated baseband signal comprise the demodulated baseband signal.

8. (Currently amended) The modulator as defined in Claim 1, wherein the second digital filter of the QDCSP further comprises:

a first register adapted to store a first value that is related to a DC offset in an in-phase portion of the received baseband signal;

a second register adapted to store a second value that is related to a DC offset in a quadrature-phase portion of the received baseband signal;

a first summing circuit adapted to combine the first value with the in-phase portion of the received baseband signal to produce an in-phase portion of a reduced offset received baseband signal;

a second summing circuit adapted to combine the second value with the quadrature-phase portion of the received baseband signal to produce a quadrature-phase portion of the reduced offset received baseband signal;

a first FIR filter adapted to receive the in-phase portion of the reduced offset received baseband signal and to generate a first in-phase portion of the demodulated baseband signal;

a second FIR filter adapted to receive a quadrature-phase portion of the reduced offset received baseband signal and to generate a second in-phase portion of the demodulated baseband signal;

a third FIR filter adapted to receive [[a]] an in-phase portion of the reduced offset received baseband signal and to generate a first quadrature-phase portion of the demodulated baseband signal;

a fourth FIR filter adapted to receive a quadrature-phase portion of the reduced offset received baseband signal and to generate a second quadrature-phase portion of the demodulated baseband signal;

a third summing circuit adapted to combine the first in-phase portion of the demodulated baseband signal with the second in-phase portion of the demodulated baseband signal to generate an in-phase demodulated baseband signal; and

a fourth summing circuit adapted to combine the first quadrature-phase portion of the demodulated baseband signal with the second quadrature-phase portion of the demodulated baseband signal to generate a quadrature-phase demodulated baseband signal, where the in-phase demodulated baseband signal and the quadrature-phase demodulated baseband signal comprise the demodulated baseband signal.

9. (Currently amended) The modulator as defined in Claim 1, wherein the second digital filter of the QDCSP further comprises:

a first FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate an in-phase demodulated baseband signal;

a second FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate a first quadrature-phase portion of the demodulated baseband signal;

a third FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a second quadrature-phase portion of the demodulated baseband signal; and

a summing circuit adapted to combine the first quadrature-phase portion of the demodulated baseband signal with the second quadrature-phase portion of the demodulated baseband signal to generate a quadrature-phase demodulated baseband signal, where the in-phase demodulated baseband signal and the quadrature-phase demodulated baseband signal comprise the demodulated baseband signal.

10. (Original) The modulator as defined in Claim 1, wherein the second digital filter of the QDCSP further comprises:

a first FIR filter adapted to receive an in-phase portion of the received baseband signal and to generate a first in-phase portion of the demodulated baseband signal;

a second FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a second in-phase portion of the demodulated baseband signal;

a third FIR filter adapted to receive a quadrature-phase portion of the received baseband signal and to generate a quadrature-phase demodulated baseband signal; and

a summing circuit adapted to combine the first in-phase portion of the demodulated baseband signal with the second in-phase portion of the demodulated baseband signal to generate an in-phase demodulated baseband signal, where the in-phase demodulated baseband signal and the quadrature-phase demodulated baseband signal comprise the demodulated baseband signal.

11. (Original) The modulator as defined in Claim 1, further comprising a coupler adapted to provide the sample signal from an output of a radio frequency amplifier, where the quadrature modulated output signal is applied as an input to the radio frequency amplifier.

12. (Original) The modulator as defined in Claim 1, further comprising a coupler adapted to provide the sample signal from the quadrature modulated output signal.

13. (Original) The modulator as defined in Claim 1, where the ACPCE circuit is configured to monitor the baseband signal and the received baseband signals in short bursts of time between about 50 microseconds to about 200 microseconds, and is further configured to store the monitored signals in a memory device.

14. (Original) The modulator as defined in Claim 1, wherein the local oscillator frequency is radio frequency (RF).

15. (Original) The modulator as defined in Claim 1, wherein the local oscillator frequency is intermediate frequency (IF).

16. (Original) The modulator as defined in Claim 15, further comprising a frequency upconverter adapted to receive a signal as an input that includes the quadrature modulated output signal, and to mix the signal with an RF signal.

17. (Original) The modulator as defined in Claim 1, wherein the ground signal switched by the termination switch is alternating current (AC) coupled to ground.

18. (Original) The modulator as defined in Claim 1, wherein the ACPCE circuit is configured to provide a test signal, and the QMCSP is configured to accept the test signal, and where the test signal includes test tones that enable the QDCSP to detect quadrature impairment characteristics.

19. (Original) The modulator as defined in Claim 1, wherein the ACPCE circuit is configured to provide updates to the first digital filter and to the second digital filter through state parameter vectors to the QMCSP and the QDCSP, respectively, to update instructions that negate the quadrature impairment.

20. (Original) The modulator as defined in Claim 19, wherein the QMCSP is adapted to activate the updates substantially simultaneously.

21. (Original) The modulator as defined in Claim 1, wherein the ACPCE circuit is configured to activate the phase shifter control signal to select the phase shift of the phase shifted output signal to measure quadrature impairment characteristics of the AQMS and the AQDS.

22. (Original) The modulator as defined in Claim 21, wherein the ACPCE circuit is configured to activate the ground switch control to characterize a DC offset corresponding to a selected phase shift.

23. (Original) The modulator as defined in Claim 1, wherein the AQDS is further coupled to a receive path from an antenna to receive a transmitted signal from an external transmitter so that the AQDS demodulates the transmitted signal.

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50. (Original) A method of quadrature modulating baseband signals comprising:

receiving an input signal in digital form, where the input signal includes both an in-phase portion and a quadrature-phase portion;

applying a first time-domain impulse response to the input signal to convert the input signal to a digital compensated signal, where the digital compensated signal substantially negates a quadrature impairment associated with a forward modulation path;

converting the digital compensated signal from digital to an analog version;

quadrature modulating, in an analog quadrature modulator, the analog version of the digital compensated signal to a quadrature modulated signal;

receiving a sample signal of the quadrature modulated signal;

applying the sample signal as an input to an analog quadrature demodulator and quadrature demodulating the sample signal to a quadrature demodulated sample signal;

converting the quadrature demodulated sample signal from analog to a digital version;

applying a second time-domain impulse response to the digital version of the quadrature demodulated sample signal to convert the digital version of the quadrature demodulated sample signal to a demodulated baseband signal, where the second time-domain impulse response substantially negates a quadrature impairment associated with a reverse demodulation path;

receiving and storing at least a portion of the input signal in a memory;

receiving and storing at least a portion of the demodulated baseband signal in the memory;

analyzing the at least portions of the input signal and the demodulated baseband signal;

characterizing the quadrature impairment characteristics associated with the forward modulation path in frequency domain by computing a first set of transfer functions of the quadrature impairments;

computing a second set of transfer functions in frequency domain, where the second set of transfer functions comprises complements to the first set of transfer functions; and

converting the second set of transfer functions from frequency domain to produce the time domain impulse responses used in the digital filtering of the input signal and the digital version of the quadrature demodulated signal.

51. (Original) The method as defined in Claim 50, further comprising applying a ground signal as an input to the analog quadrature demodulator to detect a DC offset.

52. (Original) The method as defined in Claim 50, further comprising phase rotating a local oscillator signal applied to analog quadrature demodulator relative a local oscillator signal applied to the analog quadrature modulator to characterize the first set of transfer functions.

53. (Original) The method as defined in Claim 50, further comprising:

receiving a plurality of baseband input signals at a plurality of frequencies; and

digitally combining the plurality of baseband input signals to create the input signal.

54. (Original) The method as defined in Claim 50, further comprising:

detecting an absence of transmission by an RF amplifier associated with the input signal;

receiving an external signal transmitted by an external transmitter; and

applying the external signal as an input to the analog quadrature demodulator and demodulating the external signal.

55. (Original) The method as defined in Claim 50, further comprising:

compensating for a DC offset associated with the forward modulation path by combining the digital compensated signal with a first calculated DC offset; and

compensating for a DC offset associated with the reverse demodulation path by combining the received baseband signal with a second calculated DC offset.

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